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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,614	11/01/2001	Yuan-sheng Huang	67,200-565	8180

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EXAMINER

ALEJANDRO MULERO, LUZ L

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

5

Office Action Summary	Application No. 10/004,614	Applicant(s) HUANG ET AL.	
	Examiner Luz L. Alejandro	Art Unit 1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 February 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,5,7-12,15-19,21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7-12,15-19,21 and 22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/8/06 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 5, 7-8, 11-12, 15-17, 19 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al., U.S. Patent 5,571,366 in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061.

Ishii et al. shows the invention as claimed including a semiconductor dry etching system comprising: a plasma chamber 2; a vertically movable wafer lifter 76 to hold a semiconductor wafer in a face down processing position during plasma processing at a top of the plasma chamber, the semiconductor wafer W and the wafer lifter 76 supplied with an electrical bias (for example, 14) during plasma processing (see fig. 12 and col. 11, lines 23-40). Note that the wafer lifter is vertically movable between a lower position to an upper position, where the lower position promotes loading of the wafer to the wafer lifter, and the upper position enables the supply of the electric bias supply through the wafer chuck.

Ishii et al. does not expressly disclose that the wafer lifter is positioned at the top of the plasma chamber, has sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer, the wafer exposed from the bottom of the wafer lifter through the circular opening therein, or wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose the semiconductor wafer processing face during plasma processing. Somekh et al. discloses an apparatus which holds a workpiece 40 at the top of the chamber and a wafer lifter 76/125 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a

bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening and is exposed from the bottom of the wafer lifter through the circular opening therein (see, for example, figs. 3a-3f and 5 and their descriptions). Additionally, Brors et al. discloses an apparatus which holds a workpiece 232 at the top of the chamber and a wafer lifter 234 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening and is exposed from the bottom of the wafer lifter through the circular opening therein (see, for example, fig. 14 and its description). Therefore, in view of these disclosures, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. as to comprise the claimed wafer lifter because such a wafer lifter structure is a suitable alternative means for holding the wafer at the top of the chamber.

Regarding the wafer lifter being supplied with a bias during plasma processing, method limitation form paragraph.

With respect to claim 19, note that Ishii et al. discloses a dielectric window as the lower wall of the chamber.

With respect to the limitation that only the semiconductor wafer processing surface face down is exposed while covering a periphery and side portion of the

semiconductor wafer, the examiner respectfully points out that there is no evidence that exposing only the semiconductor processing surface face down would significantly affect the overall performance of the plasma processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made that no contaminants are expected to adhere to the sides of the wafer due to the wafer face-down structure of the apparatus. Therefore, such limitation would not lend patentability to the instant application absent the showing of unexpected results or the showing that such claimed structure would significantly affect the overall performance of the plasma processing.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al. in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3, 5, 7-8, 11-12, 15-17, 19, and 21-22 above and further in view of Uchida, U.S. Patent 5,804,027 or Ishii et al., U.S. Patent 5,795,429.

Ishii et al. '366, Somekh et al. and Brors et al. are applied as above but do not expressly disclose that the one or more coils comprise one or more electromagnetic coils coupled to an electromagnetic supply. Uchida discloses an apparatus in which electromagnetic coils 6-8 connected to respective power sources are used to generate electromagnetic fields (see, for example, fig. 3). Similarly, Ishii et al. '429 discloses an apparatus in which electromagnetic coil 106 is excited by power supply 107 to form an electromagnetic field (see, for example, fig. 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. '366 modified by Somekh et al. or Brors et al., as to comprise

one or more electromagnetic coils coupled to an electromagnetic supply since such structure is known and used in the art in order to generate electromagnetic fields.

Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii et al., U.S. Patent 5,571,366 in view of Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3, 5, 7-8, 11-12, 15-17, 19, and 21-22 above, and further in view of the Admitted Prior Art (APA).

Ishii et al., Somekh et al. and Brors et al., are applied as above but do not expressly disclose that the apparatus further comprises one or more multi-pole magnets. The APA shows a semiconductor etching system, comprising: a plasma chamber 202 in which a polymer is introduced, excess polymer forming and subsequently peeling off the inner walls of the chamber and falls down due to gravity; and an electrically biased mechanism comprising a wafer chuck 218 to hold the semiconductor wafer and a bias supply 222 to electrically bias the wafer chuck; one or more coils 210 connected to RF power 214; one or more multi-pole magnets 204/206 to cooperating with the coil to assist inducement of the varying magnetic field within the chamber; and a dielectric window 208 (see fig. 2 and paragraphs 002-0010 of the instant application, especially paragraphs 009-0010). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. modified by Somekh et al. or Brors et al., as to further comprise one or more multi-pole magnets as taught by the APA in order to assist in the generation of the varying magnetic field within the chamber.

Claims 1, 3, 5, 7-8, 10-12, 15-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ishii et al., U.S. Patent 5,571,366 and Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061.

The APA shows the invention substantially as claimed including a semiconductor etching system, comprising: a plasma chamber 202 in which a polymer is introduced, excess polymer forming and subsequently peeling off the inner walls of the chamber and falls down due to gravity; and an electrically biased mechanism comprising a wafer chuck 218 to hold the semiconductor wafer and a bias supply 222 to electrically bias the wafer chuck; one or more coils 210 connected to RF power 214; one or more multi-pole magnets 204/206; and a dielectric window 208 (see fig. 2 and paragraphs 002-0010 of the instant application, especially paragraphs 009-0010).

APA does not expressly disclose an electrically biased mechanism and wafer lifter that hold the wafer upside-down within the plasma chamber. Ishii et al. discloses a semiconductor dry etching system comprising: a plasma chamber 2 in which reaction gases are introduced and reaction product particles formed fall down due to gravity (see col. 11, lines 37-39); an electrically biased mechanism (chuck 12') to hold a semiconductor wafer in the top of the chamber (upside-down), thereby preventing particles from falling onto the wafer; and a vertically movable wafer lifter 76 to hold the wafer (see fig. 12 and col. 11, lines 23-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of the APA as to be arranged to be a face-down type apparatus comprising

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the electrically biased mechanism and wafer lifter that hold the wafer upside-down within the plasma chamber as taught by Ishii et al., because in such a way the wafer to be processed can be protected from being contaminated by particles and the like, therefore further improving the yield and the throughput.). Note that the wafer lifter disclosed by Ishii et al. is vertically movable between a lower position to an upper position, where the lower position promotes loading of the wafer to the wafer lifter, and the upper position enables the supply of the electric bias supply through the wafer chuck.

APA and Ishii et al. does not expressly disclose that the wafer lifter is positioned at the top of the plasma chamber, has sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer, the wafer exposed from the bottom of the wafer lifter through the circular opening therein, or wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose the semiconductor wafer processing face during plasma processing. Somekh et al. discloses an apparatus which holds a workpiece 40 at the top of the chamber and a wafer lifter 76/125 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening and is exposed from the bottom of the wafer lifter through

the circular opening therein (see, for example, figs. 3a-3f and 5 and their descriptions). Additionally, Brors et al. discloses an apparatus which holds a workpiece 232 at the top of the chamber and a wafer lifter 234 being positioned at the top of the chamber, having sidewalls defining a first diameter greater than the diameter of the wafer and a bottom having a circular opening therein having a second diameter less than the first diameter and less than the diameter of the wafer, and wherein the wafer periphery rests on an inner top surface of the bottom portion defining the circular opening and is exposed from the bottom of the wafer lifter through the circular opening therein (see, for example, fig. 14 and its description). Therefore, in view of these disclosures, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Ishii et al. as to comprise the claimed wafer lifter because such a wafer lifter structure is a suitable alternative means for holding the wafer at the top of the chamber.

With respect to the limitation that only the semiconductor wafer processing surface face down is exposed while covering a periphery and side portion of the semiconductor wafer, the examiner respectfully points out that there is no evidence that exposing only the semiconductor processing surface face down would significantly affect the overall performance of the plasma processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made that no contaminants are expected to adhere to the sides of the wafer due to the wafer face-down structure of the apparatus. Therefore, such limitation would not lend patentability to the instant

application absent the showing of unexpected results or the showing that such claimed structure would significantly affect the overall performance of the plasma processing.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA) in view of Ishii et al., U.S. Patent 5,571,366, and Somekh et al., U.S. Patent 5,643,366 or Brors et al., EP 0276061, as applied to claims 1, 3, 5, 7-8, 10-12, 15-19, and 21-22 above, and further in view of Uchida, U.S. Patent 5,804,027 or Ishii et al., U.S. Patent 5,795,429.

APA, Ishii et al. '366, Somekh et al., and Brors et al. are applied as above but do not expressly disclose that the one or more coils comprise one or more electromagnetic coils coupled to an electromagnetic supply. Uchida discloses an apparatus in which electromagnetic coils 6-8 connected to respective power sources are used to generate electromagnetic fields (see, for example, fig. 3). Similarly, Ishii et al. '429 discloses an apparatus in which electromagnetic coil 106 is excited by power supply 107 to form an electromagnetic field (see, for example, fig. 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of APA modified by Ishii et al. '366, Somekh et al., and Brors et al. as to comprise one or more electromagnetic coils coupled to an electromagnetic supply since such structure is known and used in the art in order to generate electromagnetic fields.

Response to Arguments

Applicant's arguments filed 2/8/06 have been fully considered but they are not persuasive.

Applicant argues that Ishii et al. fails to disclose the wafer lifter supplied with an electrical bias as claimed and the characteristics of the wafer lifter as claimed.

Regarding the wafer lifter supplied with an electrical bias, note that as shown in fig. 12, the wafer lifter contacts portions of the apparatus that are applied with electrical bias and therefore, inherently, the wafer will be supplied with electrical bias.

Concerning the characteristics of the wafer lifter, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Regarding applicant's argument that the support of Ishii et al. would likely interfere with a plasma process thereby defeating an advantage of applicant's disclosed and claimed invention, attorney's arguments cannot take the place of secondary evidence such as affidavits and declarations in the record.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine the Ishii et al. reference with that of Brors et al. and Somekh et al. is clearly stated in the rejection stated above.

Regarding the fact that fig. 14 of Brors et al. does not disclose a wafer lifter, it is clear when giving the claim its broadest reasonable interpretation that element 234 can be considered a wafer lifter since without this element it does not appear that the wafer can be supported.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

This is a RCE of applicant's earlier Application No. 10/004,614. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL**

even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luz L. Alejandro whose telephone number is 571-272-1430. The examiner can normally be reached on Monday to Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luz L. Alejandro
Primary Examiner
Art Unit 1763

February 21, 2006